Exploring Density-Reliability Tradeoffs on Nanoscale Substrates: When do smaller less reliable devices make sense?

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Abstract

It is widely recognized that device and interconnect fabrics at the nanoscale will be character-ized by an increased susceptibility to transient faults. This appears to be intrinsic to nanoscale regimes and fundamentally limits the eventual benefits of the increased device density, i.e., the overheads associated with achieving fault-tolerance may counter the benefits of increased device density – density-reliability tradeoff. At the same time, as devices scale down one can expect a higher proportion of area to be associated with interconnection, i.e., area is wire dominated. This paper theoretically explores density-reliability tradeoffs in wire dominated integrated systems. We derive an area scaling model based on simple assumptions capturing the salient features of hier-archical design for high performance systems. We then evaluate overheads associated with using basic fault-tolerance techniques at different levels of the design hierarchy. This, albeit simplified model, allows us to tackle several interesting questions: When does it make sense to use smaller less reliable devices? At what scale of the design hierarchy should fault tolerance be applied in high performance integrated systems? Our analysis reveals two critical parameters, the technology and design scaling factors, which are key to predicting the reliability requirements for emerging technologies if traditional hierarchical design continues to be used.

1 Introduction

Future integrated systems will be implemented on increasingly dense substrates. These in turn are expected to be characterized by high densities of manufacturing defects and high rates of tran-sient faults [1, 2, 3, 4]. In order to achieve a desired manufacturing yield and system reliability, engineers will have to apply defect- and fault-tolerance techniques. These techniques will nec-essarily incur overheads associated with additional circuitry and redundancy [5]. Such overheads take up area on the chip and thus increase power consumption. Thus, it is possible that the defect- and fault-tolerance overheads may grow faster than extra area afforded by the increased density of devices and wires the new technologies provide. This can happen if the reliability of the substrate drops quickly with increasing density. This paper develops a theoretical model to study when this is indeed the case.

Another key observation is that as technology scales down, the impact on area and power con-sumption of wires grows faster than that of devices (at least for high performance systems). This is supported empirically by Rent's Rule [6, 7]. It states that the number of external wires for a circuit sub-block is proportional to the size of this sub-block (e.g. in gates) to the power r where r is referred to as Rent's exponent and is typically about 0.6-0.7 for high performance systems. Rent's Rule can be viewed as arising from consistency across design hierarchy levels – i.e., reflects a design style based on interconnection of increasingly complex sub-blocks. The exponent may

vary from system to a system (or sometimes even within a given system at different levels of hierarchy) reflecting not only design style, but also, the type of functionality being implemented. When Rent's exponent is greater than 0.5 for a 2D circuit, then the density of wires increases with system size growth provided that gates are tightly packed. This is reflected in the increase in metallization layers used for chips over the last decades – from 1 to 10 or more layers in today modern chips. It is technologically problematic to continue increasing the number of layers, so at some point it will become impossible to pack devices tightly due to the area required for wiring. At that point a chip's area will be wire dominated.

In such regimes (dynamic) power consumption may also be wire dominated. Indeed, static power consumption depends mostly on device physics, while dynamic power consumption is roughly proportional to load capacitance which already is dominated by wires in modern technologies. For example [8] consider a 3D design where devices were stacked vertically in 4 planes and show that the major effect is a reduction in wire length accompanied by a dramatic reduction in power consumption. Thus to understand the fundamental characteristics of future technologies, one must properly reflect wires' increasingly dominant influence on area, power and even performance.

In this paper we consider substrate technologies that are capable of delivering a high density of devices and wires but along with higher defect densities and transient fault rates. In Section 2 we propose and analyze an area scaling model for such technologies based on several natural assumptions. The model exhibits how area grows with complexity of the system (number of gates) in a wire dominated regime. Using this scaling model we consider the overheads associated with achieving fault-tolerance by applying spatial redundancy at different levels of system hierarchy. This simple model enables us to address two questions. When do smaller, but less reliable devices make sense, and at what level of the design hierarchy should fault tolerance be applied? The main contribution of this paper lies in combining a novel scaling model (capturing the wire dominated regimes of interest) with traditional reliability analysis to tackle these questions. This might be viewed in contrast to research initiated by [9] tackling computability with unreliable devices, but ignoring device and wiring overheads, see e.g., [10, 11]. By considering wire dominated regimes our work also differs from previous work considering reliability and overhead models based solely on gate count see e.g., [12]. Section 2 of this paper focuses only on gate reliability, while Section 3 motivates a general model both gates and wires may fail. This permits us to consider the manner in which device vs wire reliability impact the usefulness of a given technology. Section 4 offers some closing comments and perspective for this work.

2   Scaling Model and Basic Reliability Analysis

This section presents a novel area scaling model, capturing the wire dominated regime, which is then used to evaluate the density-reliability tradeoffs. We begin by carefully introducing several natural assumptions which underly our model.

2.1   Wire Dominated Area Scaling

The first assumption concerns interconnection across hierarchical levels. Traditional hierarchical design approaches to building increasingly complex systems are based on interconnecting sub-blocks. For example a pipelined CPU is realized based on blocks such as a fetch instruction stage, decode instruction stage, execute stage, registers file, external memory block, etc. The execute stage is itself built using different functional blocks (e.g., full word adders, multipliers, etc), where each block is built out of smaller blocks (e.g., one bit adders, etc). As a result when such systems are implemented on a substrate they lack structural regularity across hierarchical levels. By contrast, for intrinsically regular functions (e.g., memory arrays, FPGAs) one can adopt a more flat design

style where the system is comprised of a large number of simple blocks. The implementation of such systems might eventually reflect regularity in placement and routing. In this paper we focus on hierarchical designs whose eventual implementations on a substrate would exhibit 'irregular' routing and placement across levels of the hierarchy.

Assumption 2.1. *(Hierarchical consistency) We consider systems designed in a hierarchical manner across multiple levels. Hierarchical consistency in interconnecting sub-blocks at different levels means that Rent's Rule should apply. Specifically,*

$$N_{ext}(M) = k_w M^r,$$

where $N_{ext}(M)$ is number of external wires for a block with M gates (or sub-blocks) and r is Rent's exponent (typically 0.6-0.7), k_w is a proportionality constant relating external wires to number of gates to the rth power.

Following [13] we refer to Rent's Rule as satisfying *hierarchical consistency*. Indeed, consider creating a block by composing P sub-blocks each comprised of M gates. By Rent's rule each sub-block has $N_{ext}(M)$ external wires and the number of external wires for the larger block should be $N_{ext}(M)P^r$. Yet the larger block has a total of MP gates, hence the total number of external wires should also be given by

$$N_{ext}(MP) = k_w(MP)^r = (k_w M^r)P^r = N_{ext}(M)P^r,$$

which exhibits the above mentioned hierarchical consistency. Note that Rent's Rule deals with logical wires, i.e., abstract connections among blocks [6, 7]. These logical wires may be implemented using one or more physical wires. So, for example, repeaters may be inserted along a logical wire subdividing it into several physical wires. The area cost of such a logical wire will be defined as its constituent physical wires and devices used to realize it. This leads us to our second assumption.

Assumption 2.2. *(Wire area) We assume block's area is the sum of its constituent gates and wires. The area of a wire is assumed to be proportional to its length, i.e.,*

$$A_w(l) = k_l l,$$

where $A_w(l)$ denotes the area of a wire of length l and k_l is a proportionality constant.

We measure length in linear minimal gate sizes, i.e., the linear minimal gate size l_g is 1. Similarly area is measured in minimal gate areas, so that minimal area of a gate is $a_g = l_g^2 = 1$. In these units the k_l reflects average area per unit length wire in units of minimal gate area. Note however that a chip may have several metal layers that would result in a smaller coefficient k_l, e.g., 10 metal layers at best gives 10 times the area to route wires, reducing the coefficient by a factor of 10.

In general we expect Assumption 2.2 to be reasonable. A wire's area is unlikely to grow sublinearly in its length. In some cases it may grow super-linearly, e.g., if high performance is required, extra wide wires may be used to reduce resistance or extra repeaters to reduce latency. One can expect such wires to be only a small fraction which are on critical paths, and thus they would not significantly impact the overall scaling of area. As discussed in the introduction the dynamic power consumption of a wire is proportional to load capacitance, which in turn is roughly proportional to its area. Thus the total wire area can be used as a rough estimate dynamic power consumption.

The third assumption reflects our focus on hierarchically designed systems, which when mapped onto substrates exhibit irregular routing and placement.

Assumption 2.3. *(Irregular routing) The average length of wires used to interconnect sub-blocks having area A is proportional to their linear size, i.e.,*

$$L_w(A) = k_r \sqrt{A},$$

where $L_w(A)$ is the average length of wires interconnecting blocks having area A, and k_r is a proportionality constant reflecting the design's characteristics.

Note that interconnecting wires at a given scale, i.e., interconnecting blocks of a given size A, may have varying length, i.e., some may be short. Through Assumption 2.3 we posit that for systems which are hierarchically designed, resulting in irregular routing and placement, one should still expect the *average* length of such interconnections to be on the order of the linear size of the blocks they interconnect.

With these three assumptions in place one can show an area scaling law in system complexity (number of gates) capturing dominant role of wires on the area.

Theorem 2.4. *(Wire dominated area scaling) Under Assumptions 2.1-2.3 the growth in area A with system complexity M (in gates) satisfies the following differential equation:*

$$dA = \frac{A}{M}dM \;+\; k_l(k_r\sqrt{A})(k_w(1-r)M^{r-1}dM). \tag{1}$$

The solution to this equation for $r \neq 0.5$ is given by

$$A(M) = a_g(\sqrt{M} + tdM^r)^2 = a_g(M + 2tdM^{r+0.5} + (td)^2M^{2r}), \tag{2}$$

where $t = \frac{k_l k_w}{\sqrt{a_g}}$ is referred to as the technology scaling factor while $d = k_r\frac{1-r}{2r-1}$ is a design scaling factor.

We sketch the proof for Theorem 2.4 as follows. The differential growth in area represented by Eq. 1 has two terms on the right hand side. The first term can be interpreted as follows. Consider a block of area A with M gates, then the area per gate and internal wires for such a block is A/M thus if additional dM gates are added to create larger blocks, area should grow proportionally to A/M. The second term represents additional area associated with wires interconnecting blocks of size M. Consider a block of size M_2 consisting of M_2/M_1 sub-blocks of size M_1. By Rent's Rule the total number of external wires for all blocks of size M_1 is $\frac{M_2}{M_1}N_{ext}(M_1)$. This includes *some* of the internal and *all* of the external wires for the block of size M_2. However by Rent's Rule the number of external wires of the larger block is $N_{ext}(M_2)$, so the number of wires used to interconnect blocks of size M_1 within M_2 is $\frac{M_2}{M_1}N_{ext}(M_1) - N_{ext}(M_2)$. By hierarchical consistency and letting $M_2 = M + dM$ and $M_1 = M$ we obtain a differential number of interconnecting wires for blocks of size M in the form $\frac{M+dM}{M}N_{ext}(M) - N_{ext}(M + dM)$. This can be evaluated using Rent's formula. The second term also reflects our assumptions on the length and area of such wires, i.e., Assumptions 2.2 and 2.3. The solution Eq. 2 can be easily checked by substitution.

Note that the expected $A(M)$ growth includes a linear term in the number of gates, yet the other terms grow faster than linearly reflecting the dominant role of wires. Two key scaling parameters emerge. The first, called the *technology scaling factor*, depends on the average number of wires per gate k_w and wire length per linear gate length $k_l/\sqrt{a_g}$. The second, referred to as the *design scaling factor*, depends solely on characteristics of the design, i.e., on Rent's exponent r and k_r the parameter capturing the length of wires interconnecting blocks of similar size. The graph on the left in Fig. 1 exhibits the growth in area per gate, i.e., $A(M)/M$ for $d = 1$ for different technology scaling parameters; t=0.1, might be viewed as a baseline where $k_w = \sqrt{a_g}$, i.e., wire width is the same as minimal linear gate size and $k_l = 0.1$, e.g., 10 or so packed metallic layers for wiring.
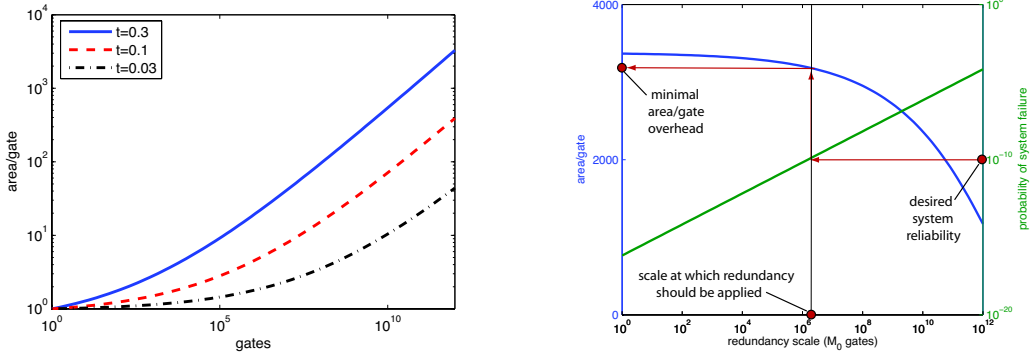
Figure 1. On the left the area $A(M)/M$ as a function of M for various technology factors and $d = 1$. On the right system overhead in area/gate and reliability as the hierarchical level at which redundancy is applied varies.

2.2 System Reliability and Fault-tolerance Overheads

To evaluate density-reliability tradeoffs, we need to characterize fault-tolerance overheads. The simplest way to achieve this is n-way spatial redundancy, i.e., replicate an unreliable sub-block n times and introduce bitwise majority voting to obtain reliable outputs. This approach achieves an exponential (in n) improvement in reliability with a linear (in n) area overhead. We recognize there are many alternatives to achieve fault-tolerance. For example, temporal redundancy requires much less overhead, but can only be applied at a sufficiently high architectural level (i.e., allowing "rollback") with blocks having sufficiently high reliability. Our motivation here is to consider high-performance, computation and/or control functions (e.g., those required to implement temporal redundancy) where spatial redundancy is a reasonable approach to achieve a significant boost reliability. We make the following assumption.

Assumption 2.5. *(Reliability and redundancy across hierarchical levels)*

a. *The probability of failure of a system is the sum of the failure probability of its constituent blocks. Thus a block of size M_0 gates has a probability of failure $p(M_0) = M_0 p_g$ where p_g is the probability of failure of a gate. Wires and voters are assumed to be reliable for now.*

b. *Spatial n-way redundancy is used to enhance a system's reliability. For a system of total size M_S gates, we assume redundancy can be applied at any of a continuum of hierarchical levels, indexed by the size of the blocks M_0, where M_0 can range from 1 to M_S gates.*

Assumption 2.5.a can be viewed as *consistency* assumption where failure probabilities are additive across constituent sub-blocks and scales. This corresponds to focusing on a regime where the failure probabilities are fairly low, and the probability of failure of a block of size M_0 gates is linear

$$p(M_0) = 1 - (1 - p_g)^{M_0} \approx M_0 p_g$$

if higher order terms can be ignored.

Assumption 2.5.b means that one may apply spatial redundancy to blocks of any size. In practice this would not be possible, but this idealization allows us to roughly investigate the granularity at which spatial redundancy should be applied. Specifically, if n-way redundancy is applied across blocks of size M_0 gates the system would have M_S/M_0 such blocks. Then for $n = 3, 5, 7 \ldots$ the

probability of failure of an n-way redundant block of size M_0 is given by

$$\sum_{i=\frac{n+1}{2}}^{n} \binom{n}{i}(1 - M_0 p_g)^{n-i}(M_0 p_g)^i \approx \binom{n}{\frac{n+1}{2}}(M_0 p_g)^{\frac{n+1}{2}}.$$

Finally using Assumption 2.5.a the probability of failure for the overall system P_S composed of $\frac{M_S}{M_0}$ such blocks is $P_S = \frac{M_S}{M_0} \times \binom{n}{\frac{n+1}{2}}(M_0 p_g)^{\frac{n+1}{2}}$.

Ignoring voters and associated circuitry, and irrespective of the block granularity M_0 at which n-way spatial redundancy is applied the overall number of gates in the system increases by a factor of n. However if replication occurs at lower levels of the hierarchy, longer wires will be required at higher levels of the design hierarchy. Indeed these wires not only get replicated n times, but also become longer taking even more area. So the total area overhead of realizing n-way spatial redundancy will be higher if it is realized at a lower level of the design hierarchy.

To properly capture these overheads when n-way spatial redundancy is applied starting at a hierarchical level M_0 we modify Eq. 1 to reflect these redundancy overheads. For $M \leq M_0$ it remains the same which by Eq. 2 gives an area $A(M_0)$ for a block of size M_0. For $M > M_0$ this is modified as follows. The initial condition becomes $M = M_0$. The initial area with n-way redundancy at scale M_0 is $nA(M_0)$. The differential growth in area for a system with n-way redundancy and $M > M_0$ is now given by

$$dA = \frac{A}{M}dM + nk_l(k_r\sqrt{A})(k_w(1 - r)M^{r-1}dM. \tag{3}$$

This can be viewed as multiplying the design scaling factor by n to capture the additional overhead associated with redundant wires.

The graph on the right in Fig. 1 shows both the area per gate and the overall system reliability when 3-way redundancy is applied to blocks M_0 ranging from a single gate to the overall system size $M_S = 10^{12}$ for a fixed probability of gate failure $p_g = 10^{-14}$. As can be seen, if redundancy is applied at a higher level M_0 one sees a lower area overhead but also a lower reliability. Thus there is a highest scale M_0 at which one can apply redundancy to achieve a given overall system probability of failure P_S. This is exhibited graphically on the plot.

Using this model we can consider if it is worth moving to smaller less reliable gates. Consider a system of fixed complexity (number of gates without redundancy) $M_S = 10^{12}$ to be implemented on a fixed absolute area, with the fixed acceptable overall probability of failure $P_S = 10^{-16}$. Given we are using n-way redundancy, we can ask what is the maximum acceptable probability of gate failure p_g such that the overheads associated with reaching the desired P_S fit in the absolute area of interest. As we reduce gate size (area) a_g, i.e., increase the density of a technology, we expect to be able to afford higher overheads for fault-tolerance, allowing higher probabilities of gate failure. The left plot on the Fig. 2 exhibits curves for the maximum tolerable probability of failure for different gate sizes and different degrees of n-way redundancy. Horizontal axis on this graph is linear size of gates measured with respect to size of bigger gates of area a_{g0} that would give the same total system area if no redundancy is applied. Such big gates should have probability of failure p_g at most $P_S/M_S = 10^{-28}$ to provide target system reliability P_S. Note that exhibited curves have a finite domain representing what is possible when M_0 ranges from 1 to M_S.

These curves reflect limits on the reliability of gates, i.e., where the redundancy overheads to achieve overall system reliability consumes all extra area afforded by reduced gate size. All points below (better system reliability) and left (less area) from any point of these curves are acceptable. Points right or above all points of these curves are unacceptable, because system built using smaller
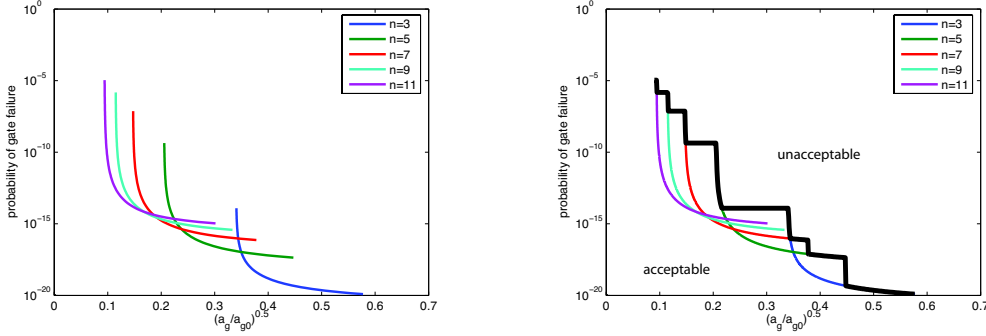
Figure 2. Minimum affordable gate reliability for reduced device size.

less reliable gates will occupy more area than non-redundant system built using bigger reliable gates. The right plot on the Fig. 2 shows the acceptable region for the various levels of redundancy.

3 Generalized Scaling Model

The results obtained in the previous section were predicated on both voters and wires being perfectly reliable. Let us reconsider these in turn. First we assumed voters can be assumed to be perfectly reliable at no cost. This is reasonable if redundancy is not applied at a very low hierarchical level. In this case each block's cost will be orders of magnitude higher than the cost of voters. Indeed, first the complexity of single bit voter is very small. Second the number of such voters is proportional to the number of external wires which by Rent's Rule scales as M^r ($r \approx 0.6 - 0.7$) which is small relative to M. Thus one could in principle use 'big' or more reliable devices to implement voters at a negligible area cost.

The second assumption that wires are reliable is harder to justify. On one hand it is likely that ionizing particles, as a source of soft faults, are more likely to impact active device areas than signals across wires. However it is not clear whether wires in emerging technologies might not also be vulnerable to ionizing particles. If this were the case, then a reasonable model would be a probability of wire failure which is proportional to its length (or equivalently its area). On the other hand it is widely recognized that other internal sources of transient errors are of critical concern. For example coupling among wires is data dependent and might be modeled as a probability of failure which is proportional to wire length. Also, delay variability, in some cases may be data dependent [1] and might again be modeled as a random event. Though in this case, it is not clear that the probability of failure is proportional to wire length, it is true that a longer wire would have a higher probability of failure. To better capture concerns with the reliability of wires and investigate their importance relative to gate reliability we shall revise Assumption 2.5 as follows.

Assumption 3.1. *(General reliability and redundancy across hierarchical levels)*

a. *The probability of failure of a system is the sum of the failure probability of its constituent blocks. A block of size M_0 gates and total wire length L_0 has a probability of failure $p(M_0) = M_0 p_g + L_0 p_w$ where p_g is the probability of failure of a gate and p_w is the probability of failure of a wire per unit length. Voters are assumed to be reliable.*

b. *Spatial n-way redundancy is used to enhance a system's reliability. For a system of total size M_S gates, we assume redundancy can be applied at any of a continuum of hierarchical levels, indexed by the size of the blocks M_0 where M_0 can range from 1 to M_S gates.*

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[1]For example the critical path in an adder becomes important only for rare inputs resulting in carries having to be propagated across the entire word.
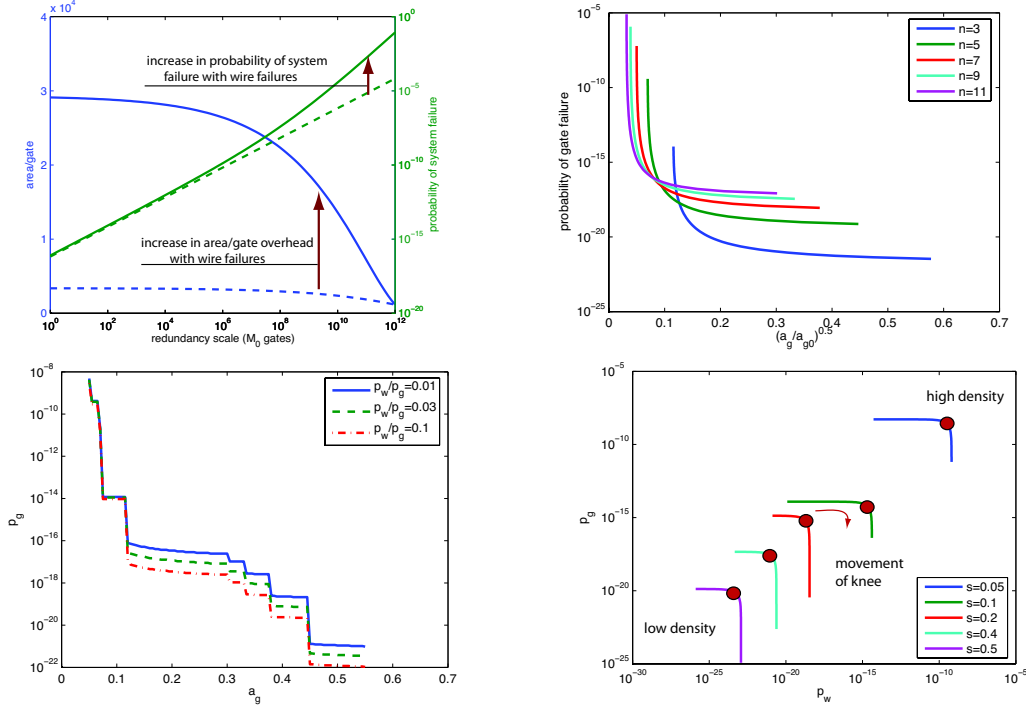
Figure 3. Top left, system overhead in area/gate and reliability as the hierarchical level which redundancy is applied varies. Top right and left bottom minimum affordable reliability for reduced device size. Bottom right, tradeoff between gate reliability (p_g) and wires reliability (p_w) at different reduced device sizes $s = (a_g/a_{g0})^{0.5}$.

c. *When redundancy is applied at level M_0 we assume that 'long' wires, i.e., interconnecting blocks of size M_0 or above are made reliable but have greater area per unit length by factor k_o.*

The key idea underlying this assumption is as follows. When spatial redundancy is applied at a certain scale, i.e., blocks of size M_0. 'Short' wires within the block are assumed to have a probability of failure which is linear in their length, and contribute to the block's failure. However 'long' wires that interconnect blocks of size M_0 and above, end up being too long and unreliable, i.e., reliability becomes wire dominated. Thus it makes sense to make long wires reliable. This can be achieved by dividing a wire into shorter sections and applying redundancy to these sections. Or possibly making long wires wider introduce a wider spacing among wires to reduce coupling. In either case making long wires reliable comes at some additional area overhead which in our assumption is modeled by the factor k_o. As in the previous section this increases design scaling factor d by a factor k_o in Eq 2. For example in the results below it is $k_0 = 3$ assuming 3-way redundancy is applied to sections of a long wire.

The top left graph in Fig. 3 exhibits the area/gate overhead and system reliability under our general model where redundancy is applied at different hierarchical levels M_0 and fixed $p_g = 10^{-14}$ and p_w ($p_w/p_g = 0.03$). For contrast, basic model (previously shown in Fig. 1) is included showing the dramatic impact of unreliable wires on overheads and system reliability. The top right graphs in the figure exhibit the new maximum possible probability of failure per gate that can be afforded as minimal device size gets smaller with respect to minimal size of reliable device. The bottom left graph shows only the bounding curves, but it does this for several rations p_w/p_g. These are akin to the results Fig. 2 for the basic model. Finally the graph on the bottom right shows maximum affordable probability of failure for gates (p_g) and wires (p_w) for various device scales. As can be

seen in the figure that knee of curves moves to the right as we increase density (the total range of ratio p_w/p_g is fixed to $10^{-6} - 10^2$). That means that for higher density reliability of wires becomes more important than reliability of gates. This could be expected as for higher densities we are increasingly in a wire dominated regime, so their reliability is increasingly a concern.

4 Conclusion

In this paper we developed a new model area scaling for wire dominated systems to study density-reliability tradeoffs for future technologies. The motivation was to evaluate when smaller less reliable devices make sense and at what hierarchical levels (granularity) one should incorporate spatial redundancy. To our knowledge this is the first attempt to evaluate such tradeoffs. Perhaps the most interesting result emerging from our work is a study of the tension between reliability of devices vs wires vs density. Our results indicate how wire reliability becomes more critical as the technology density increases. Although area can be used as a crude proxy for power, it would be interesting to further enhance the model to capture the power density issues.

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